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EXAMINER	
ZHONG, CHAD	

ART UNIT	PAPER NUMBER
2152	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,857	MODELSKI ET AL.	
	Examiner	Art Unit	
	Chad Zhong	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are presented for examination.

2. It is noted that although the present application does contain line numbers in specification and claims, the line numbers in the claims do not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning with line 1. For ease of reference by both the Examiner and Applicant all future correspondence should include the recommended line numbering.

3 Claim 17 objected under 37 CFR 1.75 as being a substantial duplicate of claim 16. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Analysis

With respect to claim 1, the examiner will interpret *instruction threads* as a sequence of instructions, this is clearly defined in applicants specification in pg 2, 1st paragraph. Specifically "Multi-thread processing divides a processing task into independently executable sequences of instructions called threads and the processor, recognizing when an instruction has caused it to be idle (i.e., first thread), switches from the instruction causing the memory latency to another instruction (i.e., second thread) independent from the former instruction.". Therefore, claim one is read as receiving two sequences of instructions, process these two sequences simultaneously within the processing pipeline. Specifically, a first instruction initially executing in a first stage and then shifted to a second stage in the pipeline. Shortly after, a second instruction will being its execution in the first stage, and moving on to the second stage upon completion of execution of first stage. The instructions are executed in a series of stages and 'pushed' forward in a series of stages, realizing a parallel processing pipeline architecture.

The pipeline itself is perceived as serial arrangement of processors or a serial arrangement of registers within a processor. Each processor or register performs part of a task/instruction and passes results to the next processor; several parts of different tasks can be performed at the same time.

Claim Rejections - 35 USC § 112, second paragraph

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The claim language in the following claims is not clearly understood, rendering the claims indefinite:

   i. As per claim 11, line 3, it is not clearly understood whether "an analysis machine" refers to "an analysis machine" in claim 6, line 1 (i.e. if they are the same, the word such as "said" or "the" must be used);

   ii. As per claim 12, line 3, it is not clearly understood whether "a packet manipulator" refers to "a packet manipulator" in claim 9, line 3 (i.e. if they are the same, the word such as "said" or "the" must be used);

   iii. As per claim 13, line 3, it is not clearly understood whether "a packet manipulator" refers to "a packet manipulator" in claim 9, line 3 (i.e. if they are the same, the word such as "said" or "the" must be used);

   iv. As per claim 13, lines 2-3, it is not clearly understood whether "an analysis machine" refers to "an analysis machine" in claim 6, line 1 (i.e. if they are the same, the word such as "said" or "the" must be used);

   iv. As per claim 14, lines 2-3, it is not clearly understood whether "an analysis machine" refers to "an analysis machine" in claim 6, line 1 (i.e. if they are the same, the word such as "said" or "the" must be used);

   v. As per claim 15, line 2, it is not clearly understood whether "an analysis machine" refers to "an analysis machine" in claim 6, line 1 (i.e. if they are the same, the word such as "said" or "the" must be used).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munson et al. (hereinafter Munson), US 2001-0037444, in view of "The RISC Concept – A Survey of Implementations", Esponda et al. (hereinafter Esponda), September 1991.

6. As per claim 1, Munson teaches a method for processing a plurality of instruction threads comprising:

retrieving a first instruction from a first thread of instructions ([0043], [0045], [0052-0053] wherein the instructions are being fetched sequentially in FIFO and being forwarded to the pipeline, which in light of the specification is a sequence of instructions. Referring to [0052], wherein the instructions are of specific length and are being stored in a FIFO queue, the instructions are being sent to the pipeline for further processing [0043], the top three instructions are assigned to the processing pipeline, and the remaining instructions pushes upwards awaiting for future assignment);

retrieving a second instruction from a second thread of instructions ([0043], [0045], Fig 5, item 520, [0052], wherein the second instruction comes after the first instruction);

Munson does not explicitly teach:

executing the first instruction in a first stage of a processing pipeline; and

forwarding the first instruction to a next stage of the processing while forwarding the second instruction to the first stage of the processing pipeline such that the first instruction and the second instruction can be executed simultaneously in the processing pipeline.

However, Esponda teaches:

executing a first instruction in a first stage of a processing pipeline (pg 4, "3. The RISC Concept", line 1-15; pg 5, lines 1-10, first instruction being *instruction i*, and first stage being *instruction fetch*); and

forwarding the first instruction to a next stage of the processing while forwarding the second instruction to the first stage of the processing pipeline such that the first instruction and the second instruction can be executed simultaneously in the processing pipeline (pg 4, "3. The RISC Concept", line 1-15; pg 5, lines 1-10, wherein 2nd instruction is *instruction i+1*, and first instruction is forwarded to the next stage *decode* while *instruction i+1* is being fetched into *instruction fetch* stage, it should be noted that the cycles of the processor is controlling which instructions gets executed). It would have been obvious to the person of ordinary skill in the art at the time of the invention to combine teachings of Munson and Esponda because teaching of Esponda to include multiple stages within the pipeline achieving parallel execution of instruction threads would improve the efficiency of Munson by allowing for execution of instruction by a factor of three (Esponda, pg 5, lines 1-5).

7. As per claim 5, Munson and Esponda teach an apparatus for processing a plurality of instruction threads ([0052]), said apparatus comprising:

a processing pipeline (Munson, Fig 5, item 540) including coupled to receive and process the plurality of instruction threads ([0052]).

Munson does not explicitly teach:

Plurality of stages within a pipeline and during a processing period, each of the plurality of stages of the processing pipeline is operating on a different one of the instruction threads from the plurality of instruction threads.

However, Esponda teaches plurality of stages within a pipeline, and during a process period, each of the plurality of stages of the processing pipeline is operating on a different one of the instruction threads from the plurality of instruction threads (pg 4, "3. The RISC Concept", line 1-15; pg 5, lines 1-10,

first instruction being *instruction i*, and first stage being *instruction fetch* ; pg 4, "3. The RISC Concept", line 1-15; pg 5, lines 1-10, wherein 2nd instruction is *instruction i+1*, and first instruction is forwarded to the next stage *decode* while *instruction i+1* is being fetched into *instruction fetch* stage, it should be noted that the cycles of the processor is controlling which instructions gets executed). It would have been obvious to the person of ordinary skill in the art at the time of the invention to combine teachings of Munson and Esponda because teaching of Esponda to include multiple stages within the pipeline achieving parallel execution of instruction threads would improve the efficiency of Munson by allowing for execution of instruction by a factor of three (Esponda, pg 5, lines 1-5).

8. Claims 2-4 and 6-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munson, Esponda, as applied to claims 1 and 5 above, and further in view of Epps et al. (hereinafter Epps), US 6,813,243.

9. As per claim 2, Munson - Esponda disclose the claim substantially, but does not explicitly teach:

transferring data from an input buffer to a packet task manager;

dispatching the data from the packet task manager to an analysis machine;

classifying the data in the analysis machine; and

modifying and forwarding the data in a packet manipulator.

However, Epps teaches:

transferring data from an input buffer (Fig 2, item 215) to a packet task manager (Fig 2, item 130, Col. 5, lines 50-55);

dispatching the data from the packet task manager to an analysis machine (Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37);

classifying the data in the analysis machine (Col. 6, lines 33-37); and

modifying and forwarding the data in a packet manipulator (Fig 4, item 450 and 460; Col. 6, lines

50-67; Col. 14, lines 1-3).

It would have been obvious to the person of ordinary skill in the art at the time of the invention to incorporate Epps teaching with of Munson, Esponda because the combination would improve the throughput rates of Munson - Esponda's systems by utilizing a software based congestion control mechanism, (Epps, Col. 3, lines 39-45).

-Epps

10. As per claim 3, Munson - Esponda disclose the invention substantially as rejected in claim 2 above, but does not teach forwarding data to output after modify. However, Epps teaches forwarding data to output after modifying (Epps, Fig. 2, item 1430; Col. 42, lines 10-21).

11. Regarding claims 4, Munson - Esponda disclose the invention substantially as rejected in claim 2 above as rejected. Munson – Esponda does not explicitly require that the data must be processed at 10GB rate, however, the processing speed is merely a matter of design choice, which depend upon the other suitable factors. The speed in which the packets are processed is inconsequential for the invention as a whole and presents no unexpected results, so long as the packet is successfully processed. Therefore, to have processing data at a rate of 10 Gbs in teachings of Munson - Esponda would have been a matter of obvious design choice to one of ordinary skill in the art.

12. As per claim 6, Munson, Esponda disclose the invention substantially as rejected in claim 5, but does not explicitly teach:

an analysis machine having multiple pipelines (Epps, Fig 4, items 410-460), wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field (Epps, Col. 6, lines 50-67; Col. 14, lines 1-3).

a packet task manager operationally connected to said analysis machine; and,

a packet manipulator operationally connected to said analysis machine.

However, Epps teaches:

a packet task manager (Epps, Fig 2, item 130, Col. 5, lines 50-55) operationally connected to said analysis machine (Epps, Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37); and,

a packet manipulator (Epps, Fig 4, item 450, 460) operationally connected to said analysis machine (Epps, Fig 4, data travel from 220 to item 450 and 460).

It would have been obvious to the person of ordinary skill in the art at the time of the invention to incorporate Epps teaching with of Munson - Esponda because the combination would improve the throughput rates of Munson - Esponda's systems by utilizing a software based congestion control mechanism, (Epps, Col. 3, lines 39-45).

13. As per claim 7, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above, including multi-threaded analysis machine (Epps, Col. 11, lines 55-65, wherein different instructions are equivalent of multi-threaded).

14. Regarding claims 8, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above. Munson – Esponda do not explicitly require that analysis machine has 32 threads, however, the amount of threads is merely a matter of design choice, which depend upon the other suitable factors. Specifically, although Munson, Esponda and Epps do not specifically disclose analysis machine has 32 threads, such limitations are merely a matter of design choice and would have been obvious in system of Munson, Esponda and Epps. Munson, Esponda, and Epps teach efficient processing of data packets within a switch through a series of pipeline stages. The limitations in claim 8 do not define a patentably distinct invention over that in Munson, Esponda, and Epps since both the invention as a whole and combination of Munson, Esponda, and Epps are directed to parallel processing of packets within a

switch. The amount of threads in which the packets are processed is inconsequential for the invention as a whole and presents no new or unexpected results, so long as the packet is successfully processed. Therefore, to have 32 threads within the analysis machine in teachings of Munson, Esponda and Epps would have been a matter of obvious design choice to one of ordinary skill in the art.

15. As per claim 9, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above, including a global access bus including a master request bus (Epps, Fig 4, item 496) and a slave request bus (Epps, Fig 4, item 497) separated from each other and pipelined (Epps, Fig 4, items 410-460).

16. As per claim 10, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above, including:

an external memory engine (Fig 4, item 215, external FIFO externally connected to analysis machine) operationally connected to said analysis machine (Epps, Fig 4, item 420, Col. 6, lines 30-35, wherein the analysis machine classifies packet data);

a hash engine (Epps, Fig. 4, item 430; Col. 24, lines 24-28) operationally connected to said analysis machine (Epps, Col. 24, lines 24-28).

17. As per claim 11, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above, including:

packet input global access bus software code (Col. 11, lines 55-60, wherein the instructions are the software code, Fig 6, item 610, 630) used for flow of data packet information from a flexible input data buffer (Epps, Fig 6, item 480) to an analysis machine (Epps, Fig 6, item 420; Col. 11, lines 55-60; Col. 6, lines 23-37, the packet header information is retrieved and processed by the pre-process stage).

18. As per claim 12, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above, including:

packet data global access bus software code (Epps, Col. 14, lines 20-27, wherein the access code is in DMA) for flow of packet data between a flexible data input bus (Epps, Fig 10, item 497) and a packet manipulator (Epps, Fig. 10, item 460, Col. 14, lines 50-67, Col 14, lines 14-16, Gather stage calculates new IP header checksum for IP packets)

19. As per claim 13, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above, including:

statistics data global access bus software code (instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates the execution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the packet manipulator) used for connection of an analysis machine (Fig 4, item 420) to a packet manipulator (Epps, Fig 4, item 460).

20. As per claim 14, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above, including:

private data global access bus software code (instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates the execution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the internal memory engine) for connection of an analysis machine (Fig 4, item 420) to an internal memory engine submodule (Epps, Fig 4, item 480, Col. 11, lines 55-65, wherein the instruction fetches

allows for connection between the PreP stage / analysis machine and the packet header buffer / internal memory engine submodule).

21. As per claim 15, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above, including:

lookup global access bus software code (instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates the execution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the internal memory engine) used for connection of an analysis machine (Fig 4, item 420) to an internal memory engine submodule (Epps, Fig 4, item 480, Col. 11, lines 55-65, wherein the instruction fetches allows for connection between the PreP stage / analysis machine and the packet header buffer / internal memory engine submodule, look up is done through pipeline control Fig 4, item 495).

22. As per claim 16 and 17, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above, including:

results global access bus software code (Epps, Col. 10, lines 5-10, the value of n is a programmable value, indicating amount of data to send to fetch stage, Fig 5, item 410) used for providing flexible access to an external memory (Epps, Col. 10, lines 5-10, amount of data received can be adjusted).

23. As per claim 18, Munson - Esponda – Epps disclose the invention substantially as rejected in claim 6 above, including:

a bi-directional access port operationally connected to said analysis machine (Epps, Col. 25, lines 1-7, wherein the input/output port are PPP/HDLC);

an input buffer (Epps, Fig 2, item 215) operationally connected to said analysis machine (input buffer operationally connected to Prep Stage Fig 4, item 420 / analysis machine through the pipeline); and

an output buffer (Epps, Fig 2, item 1430) operationally connected to said analysis machine (transmit FIFO operationally connected to Prep Stage Fig. 4, item 420 through the switch fabric).

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents and publications are cited to further show the state of the art with respect to "Multi-Packet Processor".

i. Kelsey et al. US 2003/0037228

ii. Marshall et al. US 6662252

iii. Ben-Nun et al. US 2005/0190694

iv. Flynn et al. US 5907702

v. Worrell. US 6012138

vi. Bass et al. US 2005/0243850

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chad Zhong whose telephone number is (571)272-3946. The examiner can normally be reached on M-F 7:15 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JAROENCHONWANIT, BUNJOB can be reached on (571)272-3913. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CZ
November 4, 2005

BUNJOB JAROENCHONWANIT
PRIMARY EXAMINER